AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 0001 on page 1 with the following amended paragraph.

[0001] The present invention is related to U.S. Application Serial No. 10/712,925 (Attorney ~~No. _____ (Attorney~~ Docket No. YOR20030363US1) entitled "BUILT IN SELF TEST FOR MEASURING TOTAL TIMING UNCERTAINTY IN A DIGITAL DATA PATH" to Robert L. Franch et al., filed coincident herewith and assigned to the assignee of the present invention.

Please replace paragraph 0013 on page 4 with the following amended paragraph.

[0013] Figures 1A – C show ~~1 shows~~ a block diagram of an example of a supply noise compensation circuit according to a preferred embodiment of the present invention;

Please replace paragraph 0016 on page 4 with the following amended paragraph.

[0016] Turning now to the drawings and, more particularly, Figures 1A – C show ~~1 shows a~~ block diagram ~~of an~~ examples of a supply noise compensation circuit 100 according to a preferred embodiment of the present invention. A local clock block (LCB) or clock buffer 102 receives and re-drives a global chip clock 104 into 2 complementary local clocks 106, 108. One clock, a launch clock 106, is provided as an input to a delay line 110 that is sensitive to supply voltage changes. The local clock, e.g., launch clock 106, enters the delay line 110 and, as it propagates through the delay line 110, the LCB 102 and delay line 110 mimic data propagation delay through an actual data path, e.g., in a microprocessor 122. In particular, the launch clock propagating along the delay line 110 reflects propagation delay variations resulting from switching or dI/dt noise on the circuit power supply (V_{dd}) line. Both the launch clock 106 and the second clock, a capture clock 108, clock an N bit register 112. For example, N = 129 may be convenient

for holding 3 edges worth of clock edges. The N bit register 112 latches the state of the delay line 110 as reflected at delay line taps 114. Thus, in this example the capture clock 108 captures the forward position of the timing edges in the N bit register 112. Register contents are interrogated in compare circuit 116, which locates timing edges in the delay line 110 and identifies clock cycle to clock cycle delay changes, up or down. Thus, the delay line and register 112 act as a supply noise sensor. The output of the compare circuit 116 is an input to a clock skip circuit 118, which selectively throttles back on the clock, e.g., selectively skipping one or more clocks.

Please replace paragraph 0021 on page 7 with the following amended paragraph.

[0021] Figure 2 shows an example of a section of a supply noise characterization plot 120 showing dI/dt noise in a supply line, which may be characterized as described in U.S. Application Serial No. 10/712,925 (Attorney ~~No. _____ (Attorney~~ Docket No. YOR920030363US1) entitled "BUILT IN SELF TEST FOR MEASURING TOTAL TIMING UNCERTAINTY IN A DIGITAL DATA PATH" to Robert L. Franch et al., filed coincident herewith, assigned to the assignee of the present invention and incorporated herein by reference. Upon the occurrence of a dI/dt noise spike, which typically lasts several clock cycles (e.g., anywhere from 10 – 50 cycles), the noise spike drives the supply to the delay line inverters 110 below nominal, reducing inverter switching speed and increasing inverter propagation delay, 2 – 3 register bits at about 2ns in this example 120. By the end of the next cycle at about 3.6ns in this example, the delay line slows such that the preceding edges have propagated 10 fewer stages. Also, it should be noted that the present invention has application to measurement results as described in Franch et al. and such measurements may be used to sense the onset of a dI/dt noise event to mitigate the effects of such an event in accordance with the present invention.

Please replace paragraph 0022 on page 7 with the following amended paragraph.

[0021] So for this example, instead of edges being captured at register bit locations 1, 60 and 120, by the end of the first cycle, edges are captured edges are at register bit locations 1, 58 and 116 because the noise spike slows both edges. Further, by the end of the second cycle, captured edges are at register bit locations 1, 50 and 108. Similarly, as the current responsible for the noise spike begins to fall, the supply voltage spikes positive, accelerating edge travel through delay line 110 to the point where only 2 edges (in this example) are propagating through delay line 110. A preferred embodiment integrated circuit (IC) or IC with a supply noise compensation circuit (e.g., 100 in Figures 1A – C [[1]]) senses the onset of dI/dt noise and responds by selectively skipping/forcing clock cycles to mitigate the dI/dt noise spikes and so, the extreme effects of dI/dt noise spikes.

Please replace paragraph 0023 on page 7 with the following amended paragraph.

[0023] So referring again to Figures 1A – C [[1]], when the compare 116 identifies at least a 2 bit position reduction between cycles, for example, the compare 116 sends a signal to skip control circuit 118 to block the clock for at least the next cycle. Optionally, in addition whenever, the compare 116 identifies at least a 2 bit position increase between cycles, for example, the compare 116 sends a signal to skip control circuit 118 to force the clock for at least the next cycle, i.e., preventing clock blocking for at least the next cycle. Furthermore, a single supply noise compensation circuit 100 may be located at the beginning of the chip clock tree as in the example 120 of Figure 1B, throttling the whole chip down/up in response to dI/dt noise or, supply noise compensation circuits 100 may be distributed throughout the chip clock tree as shown in the pipelined example 122 of Figure 1C, selectively throttling portions of the chip down/up in response to localized dI/dt noise.

Please replace paragraph 0024 on page 8 with the following amended paragraph.

[0024] In particular, for a complex pipelined IC such as a microprocessor 122, where chip units or blocks of logic may use localized power up/down techniques, a local supply noise compensation circuit 100 may be provided with the chip units. Each local supply noise compensation circuit 100 may selectively delay powering up/down to better distribute instantaneous chip supply demands and, thereby, reduce dI/dt noise. Also, skip driver 118 may be selected to block/force cycles until the event has subsided partially or completely (e.g., an AND of the output of compare circuit 116 with the global clock), to block/force alternate cycles or any combination thereof.

Please replace paragraph 0025 on page 8 with the following amended paragraph.

[0024] Further, a simple voltage sense may be used to sense dI/dt spikes as shown in the noise compensation circuit 130 example of Figure 3, instead of delay line 110 and register 112 of the example 100 of Figures 1A – B [[1]]. In this example, supply voltage is averaged with in an RC filter 132 and compared in voltage compare 134. A skip timer 136, e.g., a simple D-type latch, is synchronized to global clock 138 and selectively block/passes the global clock in AND gate 138. When the instantaneous supply voltage to voltage compare circuit 134 is below the average voltage at RC filter 132 by a minimum instantaneous voltage difference (d), the voltage compare circuit 134 indicates the occurrence of dI/dt noise. Upon receipt of the indication, the skip timer 136 send a block signal synchronized to global clock 138 to the AND gate 140 that blocks at least the next clock cycle. The skip timer 136 prevents spurious local clocks from occurring, e.g., from a change in the voltage compare 134 mid cycle.